Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1-13. (Canceled)

14. (Previously Presented) A method for the multichannel interpolative playback of digital waveform data samples stored in a waveform memory, comprising:

accessing said waveform memory samples from said waveform memory using an address update unit and a memory access unit;

storing two or more waveform memory samples for each channel in a cache memory;

linearly interpolating between two adjacent waveform memory samples stored in said cache memory to form a linear interpolation result; and

operating said memory access unit asynchronously from said address update unit and said linearly interpolating.

15. (Previously Presented) The method of claim 14 wherein said accessing further comprises:

incrementing a current address for each channel and addressing the waveform memory using at least a portion of said current address.

16. (Previously Presented) The method of claim 14 wherein said accessing can operate in a burst mode.

17. (Previously Presented) The method of claim 14 further comprising:

overwriting data in said cache memory for a channel that is no longer required for interpolating for a given sample point.

18. (Previously Presented) A method for implementing an interpolator for multichannel interpolative playback of digital waveform data samples stored in a waveform memory operating in waveform memory cycles, comprising:

accessing said waveform data samples in said waveform memory, said accessing including producing a bus request signal and responding to a bus acknowledge signal;

storing two or more waveform memory samples for each channel in a cache memory;

accessing two adjacent ones of said waveform memory samples from said cache memory;

linearly interpolating between said two adjacent waveform memory samples to form a linear interpolation result; and

responding to said bus request signal with memory interface logic;

producing said bus acknowledge signal with said memory interface logic; and

determining, with said memory interface logic, if said interpolator has control of the waveform memory during any given one of said waveform memory cycles.

19. (Previously Presented) A digital sampling instrument for the multichannel interpolative playback of digital waveform data samples stored in a waveform memory operating in waveform memory cycles, comprising:

a memory interface for accessing said waveform memory, including producing and responding to bus request signals and producing and responding to bus acknowledge signals, said memory interface determining if said digital sampling instrument has control of the waveform memory during any given one of said waveform memory cycles;

a cache memory storing two or more waveform memory samples for each channel;

control logic to access two adjacent ones of said waveform memory samples from said cache memory;

circuitry configured to linearly interpolate between said two adjacent waveform memory samples to form a linear interpolation result.

20. (Previously Presented) The digital sampling instrument of claim 19 further comprising memory address and control signals capable of being output disabled in response to said bus acknowledge signal.

21. (Previously Presented) The digital sampling instrument of claim 19 further comprising:

a shared bus coupling said digital sampling instrument to said waveform memory.

22. (Previously Presented) The digital sampling instrument of claim 19 wherein said control logic addresses said cache memory for read and write operations such that a write operation overwrites data for a channel that has already been read for a given sample point.

23. (Previously Presented) The digital sampling instrument of claim 22 wherein a write operation overwrites a waveform sample for the same channel.

24. (Previously Presented) The digital sampling instrument of claim 22 wherein said control logic addresses said cache memory with an address having more significant bits corresponding to a channel, and less significant bits corresponding to a portion of an address for a waveform sample for said channel.

25. (Currently Amended) A digital sampling instrument for the multichannel interpolative playback of digital waveform data samples stored in a waveform memory, the digital sampling instrument comprising:

a cache memory storing at least N waveform memory samples for each channel;

control logic to access said waveform memory samples from said cache memory; and

an interpolator configured to perform Nth order interpolation on said waveform memory samples to form an interpolation result.

26. (Previously Presented) An instrument as in claim 25 further comprising:

an address update unit; and

a memory access unit;

wherein said memory access unit operates asynchronously from said address update unit and said interpolator.

27. (Previously Presented) An instrument as in claim 25 wherein said digital sampling instrument produces a bus request signal and is responsive to a bus acknowledge signal, and further comprising:

memory interface logic responsive to said bus request signal and producing said bus acknowledge signal for determining if said digital sampling instrument has control of the waveform memory during any given one of a plurality of waveform memory cycles.

28. (Previously Presented) The digital sampling instrument of claim 27 wherein said digital sampling instrument has memory address and control signals capable of being output disabled in response to said bus acknowledge signal.

29. (Previously Presented) The digital sampling instrument of claim 25 further comprising:

a shared bus coupling said digital sampling instrument to said waveform memory.

30. (Previously Presented) The digital sampling instrument of claim 25 wherein said control logic addresses said cache memory for read and write operations such that a write operation overwrites data for a channel that has already been read for a given sample point.

31. (Previously Presented) The digital sampling instrument of claim 30 wherein a write operation overwrites a waveform sample for the same channel.

32. (Previously Presented) The digital sampling instrument of claim 25 wherein said control logic addresses said cache memory with an address having more significant bits corresponding to a channel, and less significant bits corresponding to a portion of an address for a waveform sample for said channel.

33. (Currently Amended) A method for implementing an interpolator for the multichannel interpolative playback of digital waveform data samples stored in a waveform memory, the method comprising:

accessing said waveform memory samples from said waveform memory;

storing at least N waveform memory data samples for each channel in a cache memory; and

performing Nth order interpolation on said waveform memory samples to form an interpolation result.

34. (Previously Presented) A method as in claim 33 wherein said accessing comprises:

updating addresses; and

accessing said waveform memory;

wherein said accessing said waveform memory operates asynchronously from said updating addresses and said interpolation.

35. (Previously Presented) A method as in claim 33 further comprising:

producing and responding to bus request signals with memory interface logic;

producing and responding to bus acknowledge signals with said memory interface logic; and

determining, with said memory interface logic, if said interpolator has control of the waveform memory during any given one of a plurality of waveform memory cycles.

36. (Previously Presented) A system for the multichannel interpolative playback as output samples of digital waveform data stored in a waveform memory, comprising:

coefficient logic for generating N coefficients for each channel for each of said output samples;

an interpolator circuit sharing said waveform memory with one or more other circuits, and computing a sum of N products of the contents of said waveform memory times said coefficients for each of several ones of said channels;

said interpolator circuit producing a bus request signal and responsive to a bus acknowledge signal;

memory interface logic responsive to said bus request signal and producing said bus acknowledge signal for determining if said interpolator circuit has control of the waveform memory during any given one of a pluralilty of waveform memory cycles; and

an output for providing said sum of products for each of said channels..

37. (Previously Presented) A system as in claim 36 further comprising:

a shared bus coupling said system to said waveform memory.

38. (Previously Presented) A system as in claim 36 further comprising a cache memory having a size sufficient to store two or more waveform samples for a plurality of said channels.